

U.S. Patent Application Serial No. **10/085,023**  
Amendment Under 37 C.F.R. §1.111 dated September 23, 2003  
Reply to the First Rejection of **May 23, 2003**

### **REMARKS**

Claims 1 - 9 are pending in this application, of which claims 6 - 9 have been withdrawn from consideration. By this Amendment, claim 1 has been amended and new claim 10 has been added. The applicants respectfully submit that no new matter has been added. It is believed that this Amendment is fully responsive to the Office Action dated **May 23, 2003**.

### **Allowable Subject Matter:**

Applicants gratefully acknowledge the indication on page 4 of the Action, that claim 5 would be allowable if rewritten in independent form to include all of the features of its base claim 1 and intervening claim 2.

It is respectfully submitted that newly added claim 10 includes the allowable features of claim 5 and its base claim 1 and intervening claim 2. Therefore, it is submitted that claim 10 is allowable.

### **In the Drawings**

The Examiner has requested that Fig. 8 be marked as prior art. The sheet attached herewith is a replacement sheet of drawings including Fig. 8 which has been labeled prior art. Accordingly, withdrawal of this objection to the drawings is respectfully solicited.

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**In the Specification**

The Examiner has required a new, more descriptive title. Accordingly, pursuant to the Examiner's suggestion on page 2 of the outstanding Office Action, the title has been amended to read:

**TWO-BIT SEMICONDUCTOR MEMORY WITH ENHANCED CARRIER TRAPPING**

Accordingly, withdrawal of this objection to the title is respectfully solicited.

**As to the Merits:**

As to the merits of this case, the Examiner sets forth the following rejections:

1) claims 1 and 2 stand rejected under 35 U.S.C. §102(b) as being anticipated by Eitan (U.S. Patent No. 5,768,192); and

2) claims 1 - 4 stand rejected under 35 U.S.C. §102(b) as being anticipated by Tomioka (U.S. Patent No. 5,796,140).

Each of these rejections are respectfully traversed.

In Tomioka, as indicated in Fig. 7 and its description, a memory is on the condition that it has a structure of a floating gate. That is, the memory forms a floating gate which consists of 104,

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114, and 115 (each of them is poly-silicon) in the Drawing and also it consists of a control gate 117 formed on an insulating film 116. Although, it is indicated therein that electrons are injected in 114 of the floating gate through a tunneling oxynitride film near the source/drain, electrons are not trapped in only 114 since the floating gate is a conductor and electrons spread to the entire floating gate.

Whereas, the memory of the present invention does not have a floating gate, and it traps electrons in (the high carrier trap characteristic part of) the gate insulating film.

Accordingly, Tomioka is completely different from the present invention.

In Eitan, as shown in Fig. 8B and its description, it just discloses the prior art described in the present invention as the memory structure. That is, region 68 in Fig. 8B is only indicated to describe the state that charges are trapped in a charge trap layer.

Accordingly, Tomioka and Eitan each fail to disclose or suggest the feature of the present invention that the carrier trap characteristic of the charge trap layer near the source and the drain is higher than other parts.

If, for any reason, it is felt that this application is not now in condition for allowance, the

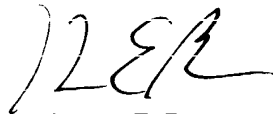
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Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



Thomas E. Brown  
Attorney for Applicant  
Reg. No. 44,450

TEB/kal  
Atty. Docket No. **020137**  
Suite 1000  
1725 K Street, N.W.  
Washington, D.C. 20006  
(202) 659-2930



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